Mindluster Platform

About the course Multi Core Computer Architecture

Multi-Core Computer course in hindi, In this course we will learn about the Multi-Core Computer architecture, parallel processing, and optimization for enhanced computing performance.

Computer Science Category's Courses

Course Lesson(49)

Lesson 1 : **Multi Core Computer Architecture Introduction Video**

Lesson 2 : **Lec 1 Review of Basic Computer Organization**

Lesson 3 : **Lec 2 Instruction Set and Addressing Modes**

Lesson 4 : **Lec 3 Instruction Encoding**

Lesson 5 : **Lec 4 Performance Evaluation Methods**

Lesson 6 : **Lec 5 Tutorial on Performance Evaluvation**

Lesson 7 : **Lec 6 Introduction to RISC Instruction Pipeline**

Lesson 8 : **Lec 7 Instruction Pipeline Hazards**

Lesson 9 : **Lec 8 Tutorial on Instruction Pipeline and Hazards**

Lesson 10 : **Lec 9 Control Hazards and Branch Prediction**

Lesson 11 : **Lec 10 MIPS Pipeline for Multi Cycle Operations**

Lesson 12 : **Lec 11 Tutorial on Longer Pipeline and Branch Prediction**

Lesson 13 : **Lec 12 Compiler Techniques to Explore ILP**

Lesson 14 : **Lec 13 Dynamic Scheduling to Explore ILP**

Lesson 15 : **Lec 14 Dynamic Scheduling with Tomasulo s Algorithm**

Lesson 16 : **Lec 15 Dynamic Scheduling with Speculative Execution**

Lesson 17 : **Lec 16 Tutorial on Static and Dynamic Scheduling**

Lesson 18 : **Lec 17 Advanced Pipelining Superscalar Processors**

Lesson 19 : **Lec 18 Introduction to GPU architectures**

Lesson 20 : **Lec 19 Case study on GPU architectures**

Lesson 21 : **Lec 20 Tutorial on Superscalar processors and GPU**

Lesson 22 : **Lec 21 Introduction to Cache Memory**

Lesson 23 : **Lec 22 Block Replacement Techniques Write Strategy**

Lesson 24 : **Lec 23 Design Concepts in Cache Memory**

Lesson 25 : **Lec 24 Optimization Techniques in Cache Memory**

Lesson 26 : **Lec 25 Advanced Cache Optimization Techniques**

Lesson 27 : **Lec 26 Tutorial on Advanced Concepts in Cache Memory 1**

Lesson 28 : **Lec 27 Tutorial on Advanced Concepts in Cache Memory 2**

Lesson 29 : **Lec 28 Cache coherence and memory consistency**

Lesson 30 : **Lec 29 Design Space for snooping protocols**

Lesson 31 : **Lec 30 Directory Based Cache coherehce**

Lesson 32 : **Lec 31 Cache coherence in multiprocessor design T**

Lesson 33 : **Lec 32 Introduction to DRAM System**

Lesson 34 : **Lec 33 DRAM Controllers Address Mapping**

Lesson 35 : **Lec 34 Secondary Storage Systems**

Lesson 36 : **Lec 35 Design Concepts in Storage Systems**

Lesson 37 : **Lec 36 Introduction to Tiled Chip Multicore Processors**

Lesson 38 : **Lec 37 Routing Techniques in Network On Chip**

Lesson 39 : **Lec 38 Network On Chip Router Micro Architecture**

Lesson 40 : **Lec 39 Concepts in Network on Chip**

Lesson 41 : **Lec 40 Energy Efficient Bufferless NoC Routers**

Lesson 42 : **Lec 41 Sidebuffered Deflection Routers**

Lesson 43 : **Lec 42 Concepts in Deflection Routers T**

Lesson 44 : **Lec 43 QoS of NoC and Caches in TCMP Systems**

Lesson 45 : **Lec 44 Emerging Trends in Network On Chips**

Lesson 46 : **Lec 45 Domain Specific Accelarators**

Lesson 47 : **Lec 46 Introduction to VEGA Microprocessors Case Study**

Lesson 48 : **Lec 47 Concepts in TCMP Systems**

Lesson 49 : **Lec 48 How to Explore Computer Architecture**

Related courses

Linear Algebra for Computer Scientists

Insertion Sort

Bubble Sort

GCSE Computer Science

Random Access Memory

Binary Trees



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