Mindluster Platform

# About the course dataflow modeling Basics

dataflow modeling course, in this course, Dive into dataflow modeling techniques, understanding data processes, and optimizing workflows.

**Computer Science Category's Courses**

# Course Lesson(28)

Lesson 1 : **System Design Through VERILOG Intro Video**

Lesson 2 : **Lec 1 Verilog Operators and Modules**

Lesson 3 : **Lec 2 Verilog Ports Data types and Assignments**

Lesson 4 : **Lec 3 Basics of gate level modeling**

Lesson 5 : **Lec 4 Half adder full adder and ripple carry adder**

Lesson 6 : **Lec 5 Parallel adder subtractor**

Lesson 7 : **Lec 6 Multiplier and comparator**

Lesson 8 : **Lec 7 Decoder encoder and multiplexer**

Lesson 9 : **Lec 8 Demultiplexer read only memory**

Lesson 10 : **Lec 9 Review of flip flops**

Lesson 11 : **Lec 10 Verilog modeling of flip flops**

Lesson 12 : **Lec 11 Modeling of CMOS gates and Boolean functions**

Lesson 13 : **Lec 12 Modeling using transmission gates CMOS dalay times**

Lesson 14 : **Lec 13 Signal strengths**

Lesson 15 : **Lec 14 Basics of dataflow modeling**

Lesson 16 : **Lec 15 Examples of dataflow modeling**

Lesson 17 : **Lec 16 Basics of behavioral modeling**

Lesson 18 : **Lec 17 Examples of behavioral modeling**

Lesson 19 : **Lec 18 Verilog modeling of counters**

Lesson 20 : **Lec 19 Verilog modeling of sequence detector**

Lesson 21 : **Lec 20 Verilog modeling FSMs and shift registers**

Lesson 22 : **Lec 21 Combinational circuit examples**

Lesson 23 : **Lec 22 Sequential circuit examples**

Lesson 24 : **Lec 23 Arithmetic and Logic Unit ALU**

Lesson 25 : **Lec 24 Static RAM and Braun Multiplier**

Lesson 26 : **Lec 25 FIR filter implementation**

Lesson 27 : **Lec 26 Baugh Wooley signed multiplier architecture**

Lesson 28 : **Lec 27 IIR filter implementation**

# Related courses

**Linear Algebra for Computer Scientists**

**Insertion Sort**

**Bubble Sort**

**GCSE Computer Science**

**Random Access Memory**

**Binary Trees**

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