Mindluster Platform

About the course VLSI Physical Design basics

VLSI Physical Design course in hindi, in this course explores the intricacies of chip layout, placement, and routing for efficient and high-performance integrated circuit design

Engineering Category's Courses

Course Lesson(67)

Lesson 1 : **PD Lec 1 Introduction to Physical Design | Tutorial | VLSI**

Lesson 2 : **PD Lec 2 CMOS Basics part 1 | Tutorial | VLSI | Physical Design**

Lesson 3 : **PD Lec 3 CMOS Basics part 2 | Tutorial | VLSI | Physical Design**

Lesson 4 : **PD Lec 4 CMOS Basics part 3 | Tutorial | VLSI | Physical Design**

Lesson 5 : **PD Lec 5 Logic Gate Conversion | Tutorial | VLSI | Physical Design**

Lesson 6 : **PD Lec 6 CMOS basics part 4 | Tutorial | VLSI | Physical Design**

Lesson 7 : **PD Lec 7 Physical Design Inputs Overview | Tutorial | VLSI | Physical Design**

Lesson 8 : **PD Lec 8 Netlists | PD Inputs part 2 | VLSI | Physical Design**

Lesson 9 : **PD Lec 9 Timing Library | libs | PD Inputs part 3 | VLSI | Physical Design**

Lesson 10 : **PD Lec 10 LEF File | PD Inputs part 4 | VLSI | Physical Design**

Lesson 11 : **PD Lec 11 Constraints File | PD Inputs part 4 | VLSI | Physical Design**

Lesson 12 : **PD Lec 12 Technology File | Tech File | PD Inputs part 5 | VLSI | Physical Design**

Lesson 13 : **PD Lec 13 DEF File | PD Inputs part 6 | VLSI | Physical Design**

Lesson 14 : **PD Lec 14 Import Design | Milky Way Library | VLSI | Physical Design**

Lesson 15 : **PD Lec 15 Floor planning part 1 | VLSI | Physical Design**

Lesson 16 : **PD Lec 16 Floor planning part 2 | VLSI | Physical Design**

Lesson 17 : **PD Lec 17 Floorplanning IO Placement part 3 | VLSI | Physical Design**

Lesson 18 : **PD Lec 18 Macro Placement Floor planning part 4 | VLSI | Physical Design**

Lesson 19 : **PD Lec 19 Macro Placement Guidelines Floor planning part 5 | VLSI | Physical Design**

Lesson 20 :
PD Lec 20 Macro Channel Spacing Estimation Floor planning part 6 | VLSI | Physical Design

Lesson 21 : **PD Lec 21 Macro Placement Guidelines Floor planning part 7 | VLSI | Physical Design**

Lesson 22 : **PD Lec 22 Blockages and Keep out Margin | Floor planning | VLSI | Physical Design**

Lesson 23 : **PD Lec 23 Macro placement issues | | Floor planning | VLSI | Physical Design**

Lesson 24 :
PD Lec 24 Power planning and power mesh creation| Floor planning | VLSI | Physical Design

Lesson 25 : **PD Lec 25 Physical Only Cells | Floor planning | VLSI | Physical Design**

Lesson 26 : **PD Lec 26 Sanity Checks 1 | Floor planning | VLSI | Physical Design**

Lesson 27 : **PD Lec 27 Sanity Checks 2 | Floor planning | VLSI | Physical Design**

Lesson 28 : **PD Lec 28 Sanity Checks 3 | Floor planning | VLSI | Physical Design**

Lesson 29 : **PD Lec 29 Cell Orientation and Flipping | Placement | VLSI | Physical Design**

Lesson 30 : **PD Lec 30 Interview Questions | VLSI | Physical Design**

Lesson 31 : **PD Lec 31 Introduction to Placement | VLSI | Physical Design**

Lesson 32 : **PD Lec 32 Placement of std cells | VLSI | Physical Design**

Lesson 33 : **PD Lec 33 Placement and Optimization | VLSI | Physical Design**

Lesson 34 : **PD Lec 34 place opt understanding | VLSI | Physical Design**

Lesson 35 : **PD Lec 35 Scan Chain Optimization | VLSI | Physical Design**

Lesson 36 : **PD Lec 36 Cell Density of std cells | VLSI | Physical Design**

Lesson 37 : **PD Lec 37 Pin Density of std cells | VLSI | Physical Design**

Lesson 38 : **PD Lec 38 Global Route Congestion | VLSI | Physical Design**

Lesson 39 : **PD Lec 39 CMOS Latch Up | VLSI | Physical Design**

Lesson 40 : **PD Lec 40 Well Tap Cell | VLSI | Physical Design**

Lesson 41 : **PD Lec 42 SVT LVT HVT Cell variants | VLSI | Physical Design**

Lesson 42 : **PD Lec 41 Tie Cell | tie low| tie high | VLSI | Physical Design**

Lesson 43 : **PD Lec 43 Timing Fixes in placement | Part 1 | VLSI | Physical Design**

Lesson 44 : **PD Lec 44 Timing Fixes in placement | Part 2 | VLSI | Physical Design**

Lesson 45 : **PD Lec 45 Spare Cells | Physical Only Cells | VLSI | Physical Design**

Lesson 46 : **PD Lec 46 Useful Skew | Timing Fixes in placement | VLSI | Physical Design**

Lesson 47 :
PD Lec 47 concurrent clock and data optimization| CCD| Timing | placement | VLSI | Physical Design

Lesson 48 : **PD Lec 48 Interview Questions | placement | VLSI | Physical Design**

Lesson 49 : **PD Lec 49 Introduction to CTS | Clock Tree Synthesis | VLSI | Physical Design**

Lesson 50 : **PD Lec 50 Clock Tree Synthesis | CTS | VLSI | Physical Design**

Lesson 51 :
PD Lec 51 How to balance skew and latency | CTS | Clock Tree Synthesis | VLSI | Physical Design

Lesson 52 : **PD Lec 52 CTS Algorithms | CTS | Clock Tree Synthesis | VLSI | Physical Design**

Lesson 53 : **PD Lec 53 CTS Constraints | Spec File | Clock Tree Synthesis | VLSI | Physical Design**

Lesson 54 : **PD Lec 54 CTS Exceptions | Float pin | Stop Pin | Exclude Pin | VLSI | Physical Design**

Lesson 55 : **PD Lec 55 Power Dissipation in clock tree | Clock gating | CTS | VLSI | Physical Design**

Lesson 56 : **PD Lec 56 Clock Gating Checks | CGC Paths | CTS | VLSI | Physical Design**

Lesson 57 : **PD Lec 57 Clock Gate Enable Checks | CGC Paths | CTS | VLSI | Physical Design**

Lesson 58 : **PD Lec 58 Integrated Clock Gates | ICG | CTS | VLSI | Physical Design**

Lesson 59 : **PD Lec 59 Master Generated and Virtual Clocks | Type of clocks | VLSI | Physical Design**

Lesson 60 : **PD Lec 60 What is crosstalk | CTS | VLSI | Physical Design**

Lesson 61 : **PD Lec 61 Crosstalk fixes and prevention | Shielding | NDR | VLSI | Physical Design**

Lesson 62 : **PD Lec 62 CTS Analysis | VLSI | Physical Design**

Lesson 63 : **PD Lec 63 Post CTS Optimization | VLSI | Physical Design**

Lesson 64 : **PD Lec 64 Skew Groups | CTS | VLSI | Physical Design**

Lesson 65 : **PD Lec 65 Introduction to Routing | VLSI | Physical Design**

Lesson 66 : **PD Lec 66 Routing Concepts | VLSI | Physical Design**

Lesson 67 : **PD Lec 67 Global and Detail Routing | VLSI | Physical Design**

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