Mindluster Platform

# About the course Verilog VHDL Programming

Verilog VHDL course in hindi, in this course Explore the powerful hardware description languages used for digital circuit design and FPGA/ASIC development in this comprehensive course.

**Computer Science Category's Courses**

# Course Lesson(13)

Lesson 1 :
**OR Gate in Xilinx using Verilog VHDL OR Gate Verilog VHDL in VLSI by Engineering Funda**

Lesson 2 :
**AND Gate in Xilinx using Verilog VHDL AND Gate Verilog VHDL in VLSI by Engineering Funda**

Lesson 3 :
**Half Adder in Xilinx using Verilog VHDL Half Adder Verilog VHDL in VLSI by Engineering Funda**

Lesson 4 :
**Full Adder in Xilinx using Verilog VHDL Full Adder Verilog VHDL in VLSI by Engineering Funda**

Lesson 5 :
**8 to 3 Encoder in Xilinx using Verilog VHDL 8 to 3 Encoder Verilog VHDL by Engineering Funda**

Lesson 6 :
**3 to 8 Decoder in Xilinx using Verilog VHDL 3 to 8 Decoder Verilog VHDL by Engineering Funda**

Lesson 7 :
**Multiplexer in Xilinx using Verilog VHDL Multiplexer Verilog VHDL in VLSI by Engineering Funda**

Lesson 8 :
**Demultiplexer in Xilinx using Verilog VHDL Demultiplexer Verilog VHDL in VLSI by Engineering Funda**

Lesson 9 :
**BCD to Seven Segment Display in Xilinx using Verilog VHDL BCD to Seven Segment Display Verilog VHDL**

Lesson 10 :
**JK Flip Flop in Xilinx using Verilog VHDL JK Flip Flop Verilog VHDL in VLSI by Engineering Funda**

Lesson 11 :
**D Flip Flop in Xilinx using Verilog VHDL D Flip Flop Verilog VHDL in VLSI by Engineering Funda**

Lesson 12 :
**BCD Counter in Xilinx using Verilog VHDL BCD Counter Verilog VHDL in VLSI by Engineering Funda**

Lesson 13 :
**Finite State Machine in Xilinx using Verilog VHDL Finite State Machine Verilog VHDL in VLSI**

# Related courses

**Linear Algebra for Computer Scientists**

**Insertion Sort**

**Bubble Sort**

**GCSE Computer Science**

**Random Access Memory**

**Binary Trees**



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